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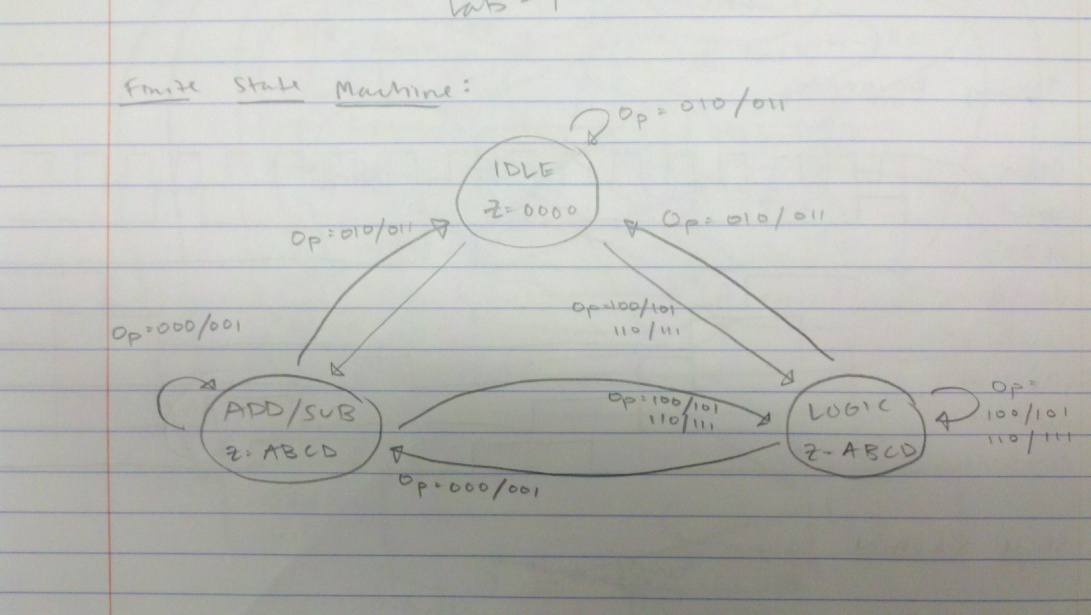
ECPE 174

Pre-Lab #7

Purpose:

This lab is intended to familiarize students with the internal memory of the FPGA. By doing so, students will need to learn how to constrain time, discover placement needed for memory, and debug any timing issues.

1. How to Connect to Internal Memory: write a paragraph about connection requirements, draw a timing diagram of the memory read and write operations (specific to your problem constraints).
2. Draw a block diagram of your overall design, making sure to label all signals and their widths; you should modify your diagram from Lab 6 to reflect both the actual ALU design used and the memory system. Write several paragraphs outlining any design decisions and assumptions including justification. Indicate how you will input and output everything on the board.
3. Design a finite state machine necessary to control the system with memory. Draw a state diagram of the FSM (MOORE)



The design may be slightly difficult to depict, but the FSM is simple. The four states are IDLE, LOGIC, ADD/SUB, and the hidden state, MEMORY. The FSM begins in the MEMORY state, and checks for the inputs “Op” which is abbreviated for operation. The MEMORY state is not depicted in the FSM diagram because an explanation of the memory state would be much easier for visualizing the FSM as a whole, rather than including another state and a plethora of arrows. Anyways, the user stores however many instructions into MEMORY, then however many times the user wishes for their instructions to run (instruction is limited to loop a maximum of 4 times).

When Op is 010 or 011, the FSM remains or returns to the IDLE stage because of invalid input. When Op is 100, 101, 110, or 111, the FSM remains or returns to the LOGIC state. When Op is 000 or 001, the FSM remains or returns to the ADD/SUB state. Now, in order to include memory, the FSM needs to run through a memory unit. This memory unit was not included in the original FSM diagram because I an explanation of the memory state would be much easier to visualize the FSM as a whole, rather than including another state and a plethora of arrows.

There are several cases left out in the state machine diagram, in the interest of time.

ENABLE NEEDS TO BE 1 TO GO TO THE LOAD STATE, IF DATA READY IS 1 THEN MEMORY TO GO TO ALU

Timing Diagram:

VHDL:

Simulation:

What inputs/outputs you need for connection requirements